FIG. 1

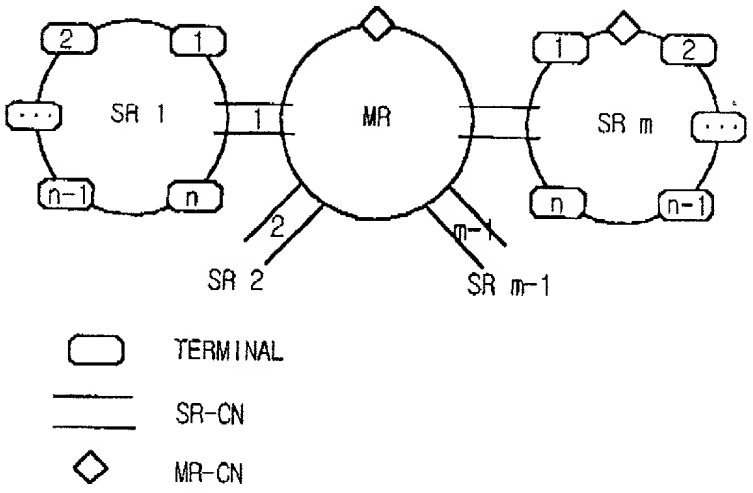

SR 1
MR
SR m
SR 2
SR m-1
TERMINAL
SR-CN
MR-CN

FIG. 3

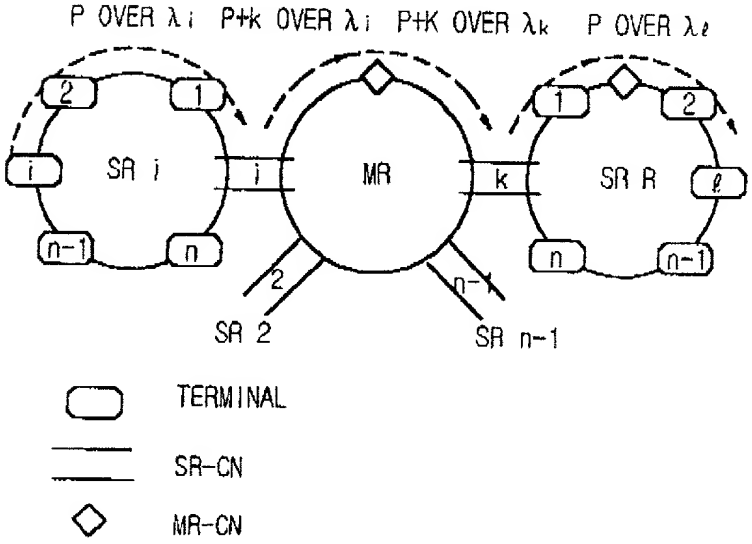

P OVER λi
P+k OVER λi
P+K OVER λk
P OVER λℓ
SR i
MR
SR R
SR 2
SR n-1
TERMINAL
SR-CN
MR-CN

FIG. 2

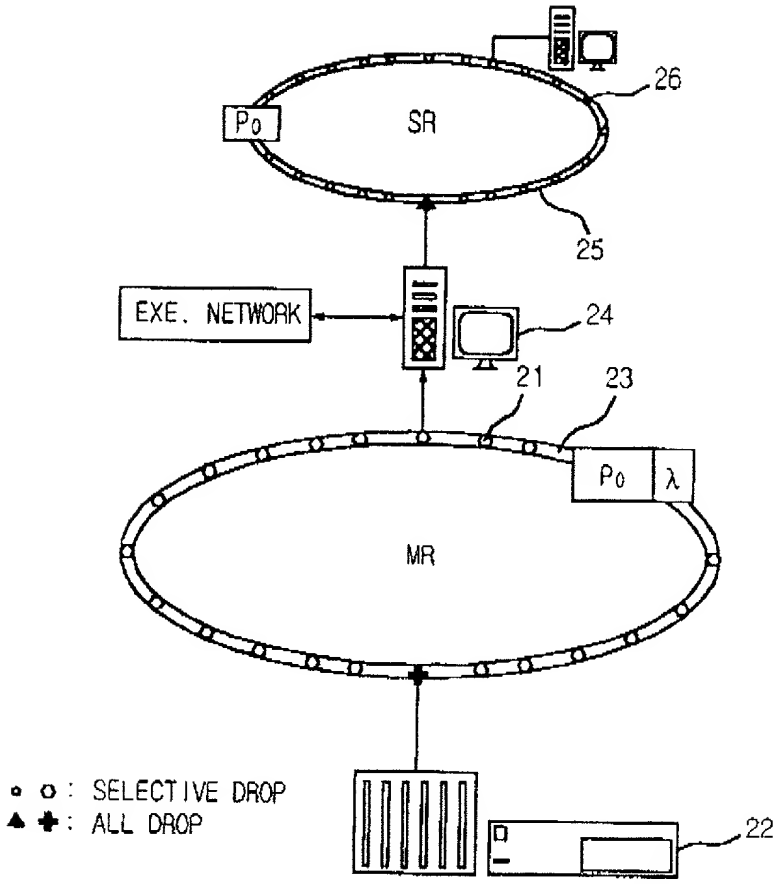

26
P0
SR
25
EXE. NETWORK
24
21
23
P0
λ
MR
SELECTIVE DROP
ALL DROP
22

FIG. 4

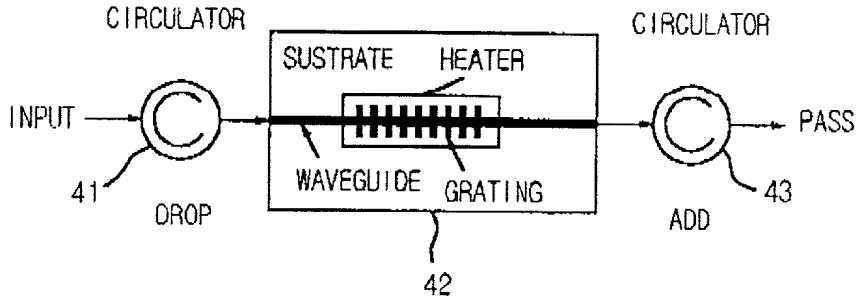

CIRCULATOR
CIRCULATOR
SUSTRATE
HEATER
INPUT
PASS
41
DROP
WAVEGUIDE
GRATING
43
ADD
42

FIG. 5

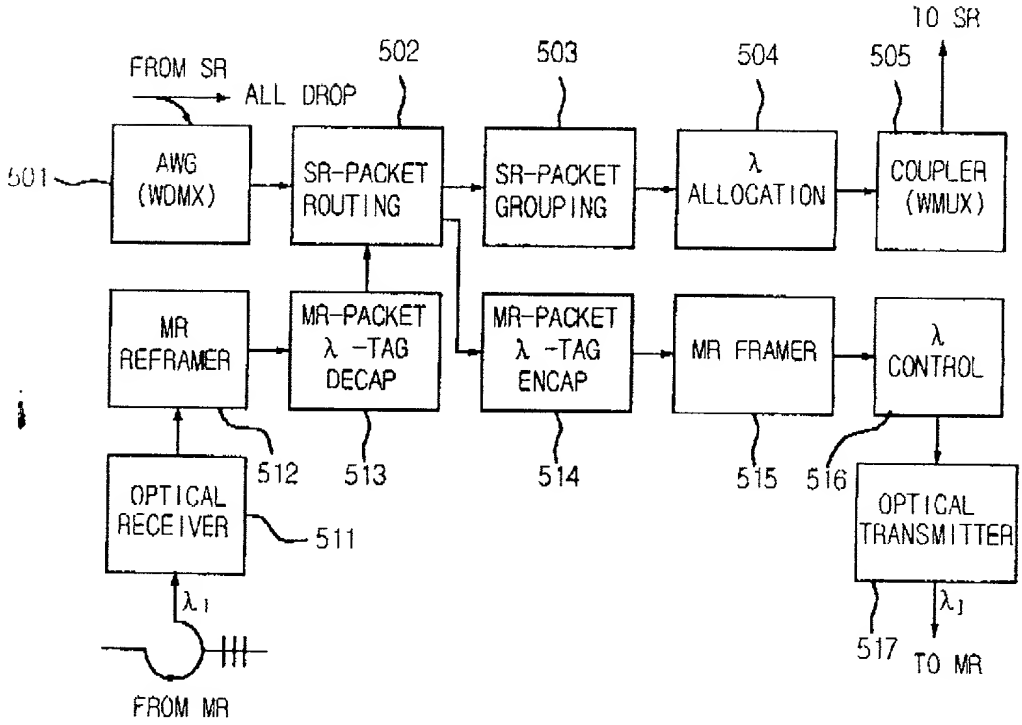
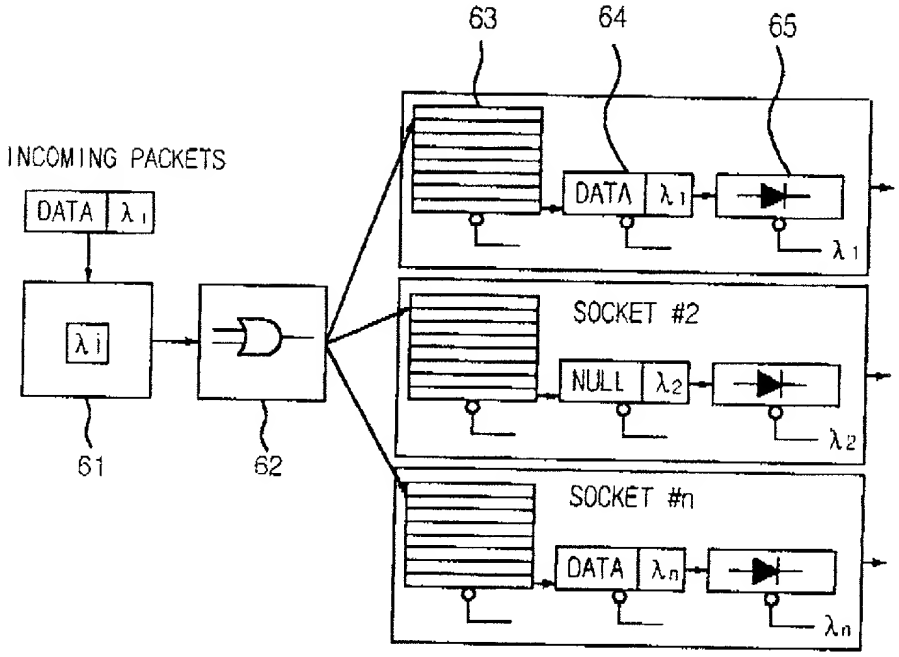

TO SR
FROM SR
ALL DROP
502
503
504
505
501
AWG (WDMX)
SR-PACKET ROUTING
SR-PACKET GROUPING
λ ALLOCATION
COUPLER (WMUX)
MR REFRAMER
MR-PACKET λ -TAG DECAP
MR-PACKET λ -TAG ENCAP
MR FRAMER
λ CONTROL
512
513
514
515
516
OPTICAL RECEIVER
511
OPTICAL TRANSMITTER
λ1
λJ
517
TO MR
FROM MR

FIG. 6


63
64
65
INCOMING PACKETS
DATA
λi
61
62
DATA
λ1
λ1
SOCKET #2
NULL
λ2
λ2
SOCKET #n
DATA
λn
λn

DOCKET NO. P2000-0050

FIG. 7

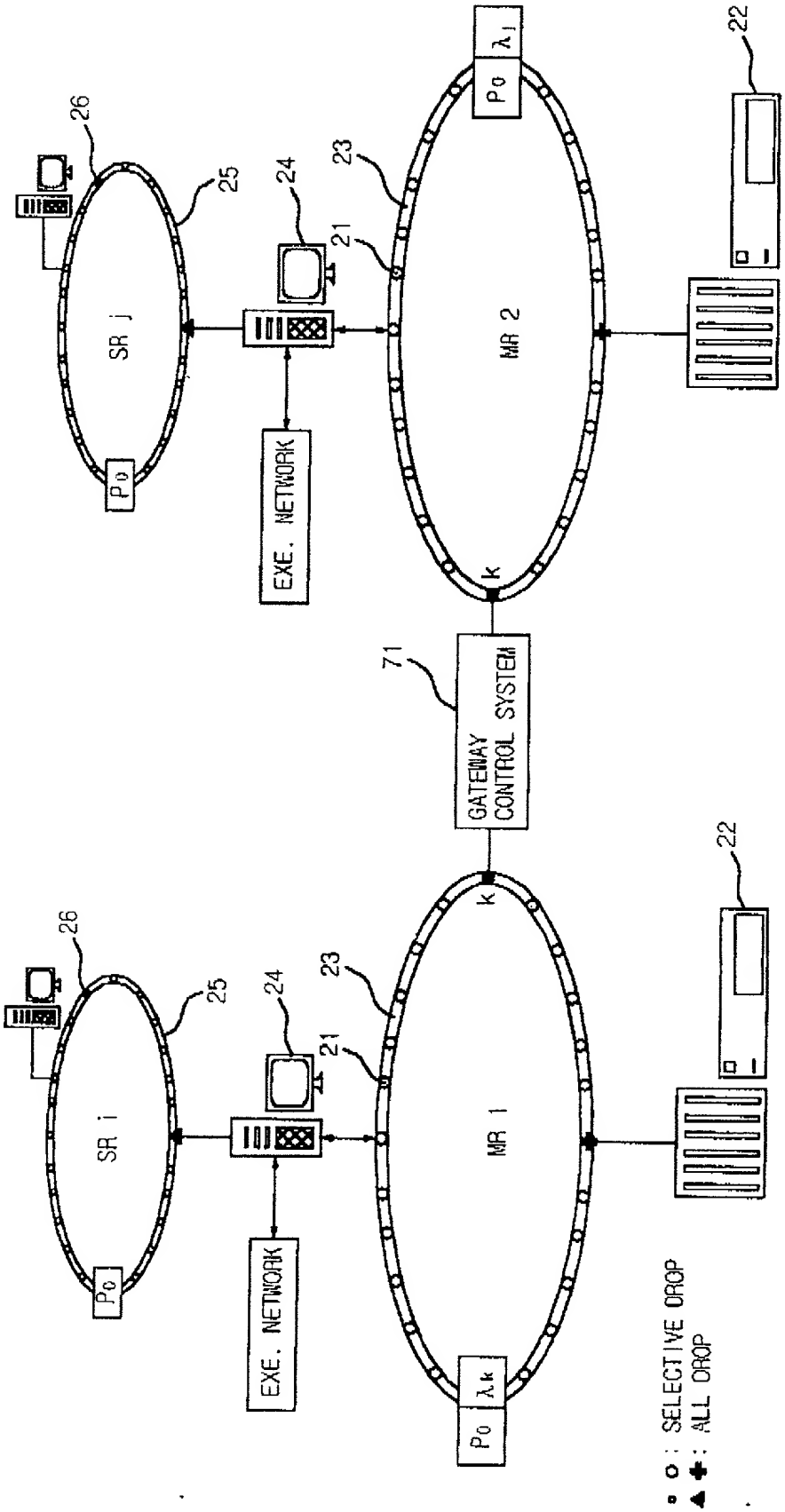
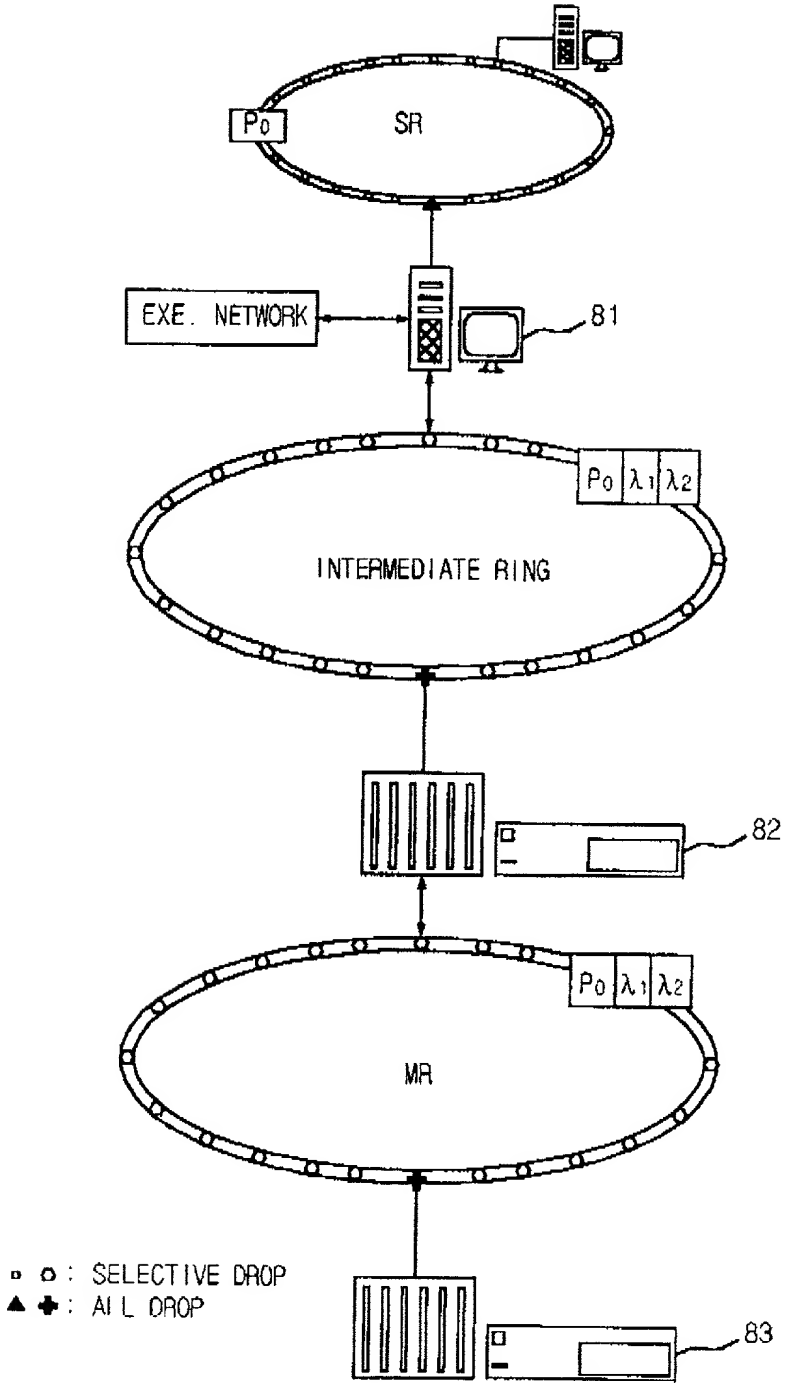


FIG. 8


P0
SR
EXE. NETWORK
81
P0 λ1 λ2
INTERMEDIATE RING
82
P0 λ1 λ2
MR
: SELECTIVE DROP
: ALL DROP
83

09/28/2001 15:57:50

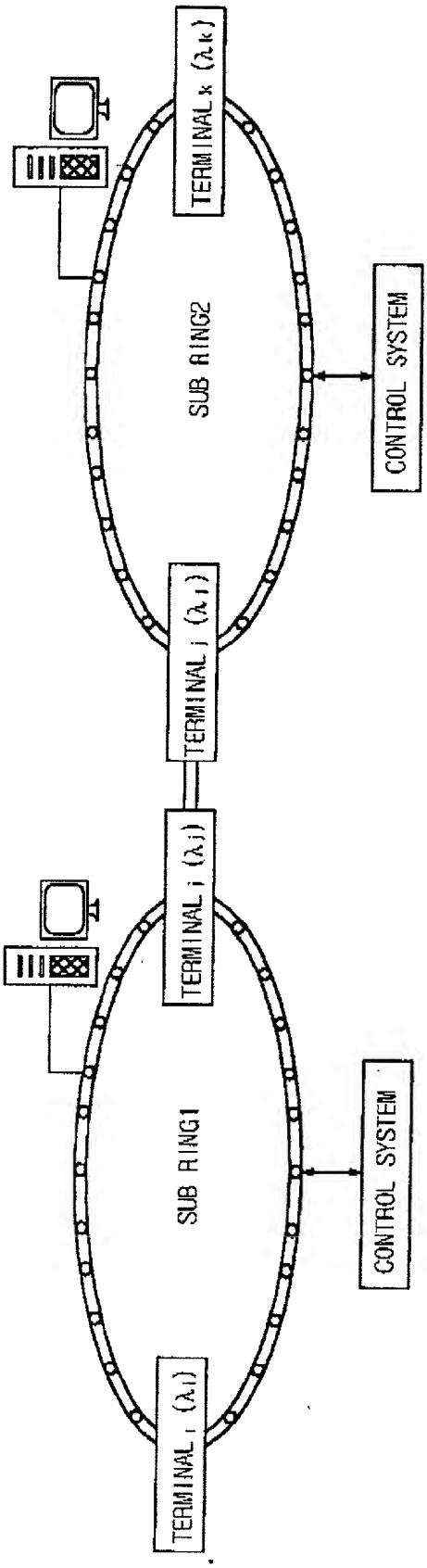


FIG. 9